

REMARKS

Claims 1-39 are pending in this application. Claims 1 and 14 have been amended. No new matter has been introduced.

Claims 1-9, 11, 13-22, 24, 26-35, 37 and 39 stand rejected under 35 U.S.C. §102(e) as being anticipated by David (U.S. Patent No. 6,068,954) (“David”). This rejection is respectfully traversed.

The claimed invention relates to a method and system for measuring the registration between integrated circuit layers. As such, amended independent claim 1 recites a “method for measuring the registration between at least two integrated circuit layers” by *inter alia* “generating a top-down image of a field of said at least two integrated circuit layers, each of said layers having a respective visible feature in said image” and “digitizing said image and processing said digitized image to determine a relative location of said visible feature of one of said layers, relative to said visible feature of the other of said layers.” Amended independent claim 1 also recites “determining if said relative location is within acceptable design limits for said integrated circuit layers.”

Amended independent claim 14 recites a “system for measuring the registration between at least two integrated circuit layers” comprising *inter alia* “an imaging system for generating a top-down image of a field of said at least two integrated circuit layers, each of said layers having a respective visible feature in said image” and “means for digitizing said image and processing said digitized image to determine a relative location of said visible feature of one of said layers, relative to said visible feature of the other of said layers.” Amended independent claim 14 also recites “means for determining if said relative location is within acceptable design limits for said integrated circuit layers.”

Independent claim 27 recites a “method for measuring the registration between integrated circuit layers” by *inter alia* “providing a first integrated circuit layer . . . comprising at least a first visible feature,” “providing a second integrated circuit layer . . . comprising at least a second visible feature” and “generating a top-down image of a field of

said first and second integrated circuit layers, including said first and second visible features.” Independent claim 27 also recites “digitizing said top-down image to provide a digitized image, and processing said digitized image to determine a relative location of said first visible feature of said first integrated circuit layer, relative to said second visible feature of said second integrated circuit layer.” Independent claim 27 further recites “determining if said relative location is within acceptable design limits for said first and second integrated circuit layers.”

David relates to a wafer alignment method. According to David, “a photomask is provided having a set of alignment pattern openings” so that “the substrate is first photoexposed through one of the set of alignment pattern openings and the circuitry openings, and not the other.” (Col. 1, lines 52-56). Davis also teaches that “[a]fter the first exposing, the substrate is second exposed through the other of the openings on the photomask” and that “a latent image of an alignment pattern is formed and received by a masking layer over a substrate.” (Col. 1, lines 56-60). In this manner, “[t]he position of the latent image of the alignment pattern is inspected relative to an underlying layer of material over the substrate” and “[a]lignment is ascertained through inspection of the latent image relative to the underlying layer of material.” (Col. 1, lines 61-64).

David fails to disclose all limitations of claims 1-9, 11, 13-22, 24, 26-35, 37 and 39. David fails to disclose, teach or suggest a “method for measuring the registration between at least two integrated circuit layers” by *inter alia* “generating a top-down image of a field of said at least two integrated circuit layers, each of said layers having a respective visible feature in said image,” as amended independent claim 1 recites. David also fails to disclose, teach or suggest “an imaging system for generating a top-down image of a field of said at least two integrated circuit layers, each of said layers having a respective visible feature in said image,” as amended independent claim 14 recites. David further fails to disclose, teach or suggest “generating a top-down image of a field of said first and second integrated circuit layers, including said first and second visible features,” as independent claim 27 recites.

David teaches that “a latent image of an alignment pattern is formed and received by a masking layer over a substrate” (col. 1, lines 56-60) and that “[t]he *position of the latent image of the alignment pattern is inspected relative to an underlying layer of material over the substrate*” (col. 1, lines 61-64), and not by “generating a top-down image” of a field of at least two integrated circuit layers,” as independent claims 1, 14 and 27 recite.

David is also silent about “digitizing said image and processing said digitized image to determine a relative location of said visible feature of one of said layers, relative to said visible feature of the other of said layers” (claims 1 and 14) or about “digitizing said top-down image to provide a digitized image, and processing said digitized image to determine a relative location of said first visible feature of said first integrated circuit layer, relative to said second visible feature of said second integrated circuit layer” (claim 27). In fact, David specifically emphasizes that “[a]lignment is ascertained through inspection of the latent image relative to the underlying layer of material” (col. 1, lines 61-64), and not by digitizing and further processing the digitized image, as in the claimed invention.

Applicants note that the assertion of the Office Action that “[t]he ‘digitizing’ is met by Davis by an implicit, if not inherent disclosure” is an unsupported assertion. “When the PTO asserts that there is an explicit or implicit teaching or suggestion in the prior art, it must indicate where such a teaching or suggestion appears in the reference The mere fact that a certain thing may result from a given set of circumstances is not sufficient [to establish inherency] ‘That which may be inherent is not necessarily known.’” In re Rijckaert, 9 F.3d 1531, 1534 (Fed. Cir. 1993) (emphasis added). The Office Action fails to support its assumption with a reference to cited prior art. Moreover, the Office Action has not alleged or shown that the assumed step is instructional to those skilled in the art. In short, the Office Action has not established that the assumed step is inherent. The step of “ascertain[ing] whether the image of alignment pattern 12 is aligned with the underlying substrate structure” in David simply does not meet the steps of

digitizing an image and then processing the digitized image for a particular subsequent determination of the present invention.

Applicants further point out that the crux of David is a wafer alignment method that employs a metrology structure such as a registration pattern or mask located in a region outside of the circuit region. For this, Davis teaches that in one embodiment “a latent image of an alignment pattern is formed and received by a masking layer over a substrate” and that “[t]he position of the latent image of the alignment pattern is inspected relative to an underlying layer of material over the substrate.” (Col. 1, lines 58-63). In this manner, “[a]lignment is ascertained through inspection of the latent image relative to the underlying layer of material.” (Col. 1, lines 63-64). On the other hand, the present invention is directed to a method of measuring registration of at least two integrated circuit layers without the use of conventional registration marks and patterns. Applicants also note that the method employed by David is similar to that described in the Background of the Invention section of the application (page 3, first full paragraph), and where Applicants point out the problems of the prior art registration measurement techniques. For at least these reasons, David fails to disclose all limitations of claims 1, 14 and 27, and withdrawal of the rejection of claims 1-9, 11, 13-22, 24, 26-35, 37 and 39 is respectfully requested.

Claims 12, 25 and 38 stand rejected under 35 U.S.C. § 103 as being unpatentable over David in view of Worster et al. (U.S. Patent No. 5,472,252) (“Worster”). This rejection is respectfully traversed.

Claims 12, 25 and 38 depend on independent claims 1, 14 and 27 and recite that the “optical system comprises a microscope and a video camera.”

Worster relates to a “laser imaging system . . . to analyze defects on semiconductor wafers that have been detected by patterned wafer defect detecting systems (wafer scanners).” (Abstract). According to Worster, “[t]he laser imaging system replaces optical microscope review stations now utilized in the semiconductor fab environment to examine detected optical anomalies that may represent wafer defects.” (Abstract). Worster

also teaches that “[i]n addition to analyzing defects, the laser imaging system can perform a variety of microscopic inspection functions including defect detection and metrology” and that “[t]he laser imaging system uses confocal laser scanning microscopy techniques, and operates under class 1 cleanroom conditions and without exposure of the wafers to operator contamination or airflow.” (Abstract).

The subject matter of claims 12, 25 and 38 would not have been obvious over David in view of Worster. Specifically, the Office Action fails to establish a *prima facie* case of obviousness. Applicants note that courts have generally recognized that a showing of a *prima facie* case of obviousness necessitates three requirements: (i) some suggestion or motivation, either in the references themselves or in the knowledge of a person of ordinary skill in the art, to modify the reference or combine the reference teachings; (ii) a reasonable expectation of success; and (iii) the prior art references must teach or suggest all claim limitations. See e.g., In re Dembiczak, 175 F.3d 994 (Fed. Cir. 1999); In re Rouffet, 149 F.3d 1350, 1355 (Fed. Cir. 1998); Pro-Mold & Tool Co. v. Great Lakes Plastics, Inc., 75 F.3d 1568, 1573 (Fed. Cir. 1996).

In the present case, neither David nor Worster, whether considered alone or in combination, teach or suggest all limitations of independent claims 1, 14 and 27. Neither David nor Worster teaches or suggests “generating a top-down image of a field of said at least two integrated circuit layers,” as amended independent claim 1 recites, or “an imaging system for generating top-down of a field of said at least two integrated circuit layers, each of said layers having a respective visible feature in said image,” as amended independent claim 14 recites. In addition, neither David nor Worster teaches or suggests “generating a top-down image of a field of said first and second integrated circuit layers, including said first and second visible features” and “digitizing said top-down image to provide a digitized image,” as independent claim 27 recites. As noted above, David fails to teach or suggest the above-noted limitations of independent claims 1, 14 and 27.

Similarly, Worster fails to teach or suggest “generating a top-down image of a field of said at least two integrated circuit layers,” “digitizing said image and processing

said digitized image to determine a relative location of said visible feature of one of said layers, relative to said visible feature of the other of said layers” and “determining if said relative location is within acceptable design limits for said integrated circuit layers,” as amended independent claim 1 recites. Worster also fails to teach or suggest “an imaging system for generating a top-down image of a field of said at least two integrated circuit layers,” “means for digitizing said image and processing said digitized image to determine a relative location of said visible feature of one of said layers, relative to said visible feature of the other of said layers” and “means for determining if said relative location is within acceptable design limits for said integrated circuit layers,” as amended independent claim 14 recites. Worster further fails to teach or suggest “generating a top-down image of a field of said first and second integrated circuit layers, including said first and second visible features” and “digitizing said top-down image to provide a digitized image,” as independent claim 27 recites. The crux of Worster is a laser imaging system that uses confocal laser scanning microscopy techniques, and not a method of generating an image of a field, digitizing the image and determining if the relative location is within design limits, as in the claimed invention.

Applicants also note that Worster teaches against the use of an “optical system” that comprises “a microscope and a video camera,” as claims 12, 25 and 38 recite. For example, in describing the laser imaging system that uses confocal laser scanning microscopy techniques, Worster specifically mentions that “[u]nlike scanning electron microscopes (SEMs) that have previously been used for defect analysis, the laser imaging system will not damage samples or slow processing, costs significantly less to implement than an SEM, can produce a three dimensional image which provides quantitative dimensional information, and allows sub-surface viewing of defects lying beneath dielectric layers.” (Abstract). Further, in describing the benefits of a laser imaging system with confocal laser scanning microscopy, Worster notes that “while SEMs can produce images with resolution on the nanometer scale, they have certain limitations.” (Col. 3, lines 38-40). Worster also emphasizes that “the laser imaging system [of Worster] has an ability the SEM cannot match: sub-surface viewing of defects lying beneath dielectric layers.” (Col. 3,

lines 57-59). Accordingly, it is clear that Worster teaches against the use of an optical system as contemplated by the claimed invention. For at least these reasons, the Office Action fails to establish a *prima facie* case of obviousness, and withdrawal of the rejection of claims 12, 25 and 38 is respectfully requested.

Claims 10, 23 and 36 stand rejected under 35 U.S.C. § 103 as being unpatentable over David in view of Seiler et al. (U.S. Patent No. 4,766,311) ("Seiler"). This rejection is respectfully traversed.

Claims 10, 23 and 36 depend on independent claims 1, 14 and 27 and recite that the "imaging system includes a scanning electron microscope."

Seiler relates to a "method and apparatus for making precise measurements as small as in submicron distances of an object or specimen (13)." (Abstract). According to Seiler, "[a]n instrument, such as a scanning electron microscope (10) scans the object (13) to obtain a first scan representation thereof" and "stage (18) is then shifted a precise known distance and a second scan is made thereof." (Abstract). Seiler also teaches that "[t]he results of the two scans are stored and compared by the microprocessor (20) to determine the apparent magnitude of the stage shift in arbitrary units."

The subject matter of claims 10, 23 and 36 would not have been obvious over David in view of Seiler. Again, the Office Action fails to establish a *prima facie* case of obviousness. As noted above, David fails to teach or suggest all limitations of independent claims 1, 14 and 27. Applicants also note that David teaches the use of "*conventional metrology tools*," such as registration patterns or marks, for visual or automated inspection of an alignment pattern, and not generating an image of a field by employing "*an imaging system*," as in the claimed invention (emphasis added). David teaches that "the image of alignment pattern 12 received by undeveloped photoresist layer 24 is inspected relative to an underlying substrate structure, which in this example comprises alignment reference mark 22" and that "[i]nspection can take place through visual inspection or automated

inspection using *conventional metrology tools*,” and not though an “imaging system,” as in the claimed invention.

In addition, Seiler teaches a precision SEM apparatus, and not “generating a top-down image of a field of said at least two integrated circuit layers,” “digitizing said image and processing said digitized image to determine a relative location of said visible feature of one of said layers, relative to said visible feature of the other of said layers” and “determining if said relative location is within acceptable design limits for said integrated circuit layers,” as amended independent claim 1 recites. Seiler also fails to teach or suggest “an imaging system for generating a top-down image of a field of said at least two integrated circuit layers, each of said layers having a respective visible feature in said image,” as amended independent claim 14 recites. Seiler is also silent about “generating a top-down image of a field of said first and second integrated circuit layers, including said first and second visible features” and “digitizing said top-down image to provide a digitized image,” as independent claim 27 recites. For at least these reasons, the Office Action fails to establish a *prima facie* case of obviousness, and withdrawal of the rejection of claims 10, 23 and 36 is also respectfully requested.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

Dated: March 29, 2004

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